4.3 A Quad 6Gb/s Multi-rate CMOS Transceiver with TX Rise/Fall-Time Control

Yongsam Moon, Gijung Ahn, Hoon Choi, Namhoon Kim, Daeyun Shim

Silicon Image, Sunnyvale, CA

The presented quad-channel transceiver incorporates a capacitance-multiplication technique for the area reduction of a thick-gate loop filter in a PLL, a programmable TX rise/fall-time control and SSC generator (SSCG) for EMI reduction, and pre-emphasis (PE) and FFE for ISI compensation. The design is fabricated in a 1P6M 0.13μm dual-gate (1.2V and 2.5V) CMOS logic process.

The designed quad-channel configuration is shown in Fig. 4.3.1. While a common TXPLL is shared by all the transmitters, a local RXPLL is dedicated to each receiver. For 6Gb/s, a 25MHz crystal is used for a low-cost design in spite of the relatively large PLL jitter induced. Due to SSC control, the spectra of the TXPLL clocks and high-speed outputs, TXP and TXN are spread. In the receiver, an FFE is followed by a dead-zone bang-bang CDR (or tracking PLL) [1], a lock detector [1] as a frequency acquisition aid, S2P for deserialization, and an elastic FIFO for frequency-tolerance compensation up to 5000ppm of SSC. To ease testing at the full speed, BIST is integrated in the chip.

0.2~0.4UI TX rise/fall time (T_{TR}) is optimal for both signal quality and EMI reduction of TXP and TXN. In multi-rate applications, one fixed T_{TR} cannot cover all data rates so T_{TR} must be controlled according to data rate. In [2], T_{TR} of the main driver can be adjusted by controlling the load of the pre-driver (C_{PRD}). However, due to the high gain of the main driver, T_{TR} is just a weak function of C_{PRD}. In [3], since serialized data goes through a DLL-controlled delay line, the operating frequency could be limited. In the proposed design, the main driver is split into multiple legs, each of which is controlled by its own pre-driver as shown in Fig. 4.3.2. For the smallest T_{TR}, all pre-drivers are biased on, while for large T_{TR} some pre-drivers can be biased off. Due to the *RC* delay among pre-drivers, biased-off pre-drivers will respond later sequentially to increase T_{TR}. To control T_{TR} according to the data rate, pre-driver bias controls, *En*[0:4], will be programmed.

The proposed FFE, as shown in Fig. 4.3.3, is modified from [4] for 4x reduction of the varactor area. The low-frequency gain is set by degeneration resistance with a thermometer-coded *lpc*[0:*N*-1] and the high-frequency boosting is set by degeneration capacitance with *hpc*[0:*N*-1]. The optimum sets of *lpc* and *hpc* are programmed by an upper layer, which will equip adaptation. When all *hpc* bits are set to be '1', the switched-C network has the maximum capacitance of C_{VAR}. The simulation result in Fig. 4.4.3 shows that the response has 6.2dB peak at 3.2GHz with C_{VAR} of 0.5pF. Since the capacitor is differentially connected, the varactor in the proposed FFE can have 4x smaller physical area with the same effective capacitance. Since varactor takes the most area of an FFE, the area can be drastically reduced so that the FFE can be integrated in the pad frame.

If a 200pF loop filter (LF) is designed with a thin-gate device in 0.13μm technology, its gate leakage current is around several tens of μA. The thick-gate device is used for the LF design in spite of the area penalty. To relax the area issue, a capacitance-multiplication scheme can be used. For example, an ideal amplifier can be utilized [5]. But, there will be a static offset current through a resistor in LF even in locked state (I_{CP}=0) due to the offset and noise of a realistic amplifier, thereby incurring large jitter. In the proposed design, instead of an amplifier, an auxiliary charge pump (CP2) is utilized, as shown in Fig. 4.3.4. While I_{CP1} flows through the resistor, the reduced current of 'I_{CP1}-I_{CP2}' flows through the capacitor, reducing the pumped charge into the capacitor. Therefore, the proposed PLL with 2 charge pumps is equivalent to the typical PLL with multiplied capacitance as shown in Fig. 4.3.4. If $I_{CP2}=\alpha \cdot I_{CP1}$, a multiplication factor is $\beta=1/(1-\alpha)$. A PFD in the PLL or a PD in CDR generates 2 pairs of UP and DOWN pulses for CP1 and CP2. However, according to the mismatch between the UP current ($I_{CP,P}$) and the DOWN current ($I_{CP,N}$) in each charge pump, it is desirable that $\alpha \geq 2/3$ so $\beta \leq 3$. The worst-case mismatch is suppressed to be <10%.

Figure 4.3.5 shows the proposed SSCG consisting of a PLL, 12-phase clock, and SSC Control. Similar to [6], the output frequency is determined by the amount of phase shift (*P*) as $Fy=Fx \cdot (60-P/12)$. The modulation frequency of SSC is set as 30kHz and the modulation amount of 5000ppm. The number of the multi-phase clocks can be determined by the allowed jitter amount and 12-phase is chosen. The *P* is dynamically changed according to a modulation profile. Although *P* has quantization noise, low-jitter clock output can be achieved with the low-pass characteristic of the PLL since a 2nd-order ΔΣ modulator shapes the noise to a higher frequency. Simulation results show that the tracking skew in RX can be lowered with higher order ΔΣ modulator and higher RXPLL bandwidth.

As shown in Fig. 4.3.6(a), 8.6Gb/s TX eye shows $2.3ps_{rms}$ and $18.7ps_{pp}$ jitter and 500mVppd output amplitude, where 35.8MHz reference clock is used and pre-emphasis is enabled. In 6Gb/s, *En* is set to "11111" and TX eye shows 50.7ps (0.3UI) T_{TR}. In 3Gb/s, *En* is "10101" and T_{TR} is 84ps (0.25UI). In 1.5Gb/s, *En* is "10001" and T_{TR} is 150ps (0.23UI). System tests show that the transceiver operates at 6Gb/s over a SATA connector and an 8m SATA cable with an attenuation of 16.2dB at 3GHz with no error detected ($BER<10^{-14}$). The 6Gb/s RX eye has little eye opening in spite of TX pre-emphasis being enabled as shown in Fig. 4.3.6(b). The recovered clock jitter is $10.9ps_{rms}$ and $133ps_{pp}$. SSCG shows 11.7dB peak reduction and 15MHz spread amount when a single 3GHz (1010) tone is observed. Fig. 4.3.7 shows the chip micrograph. The chip area is $2.4 \times 0.95mm^2$ and it consumes 386mW at 6Gb/s.

Acknowledgements:
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References:
[1] Y. Moon, et al., "A 0.6-2.5-GBaud CMOS Tracked 3× Oversampling Transceiver With Dead-Zone Phase Detection for Robust Clock/Data Recovery," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1974-1983, Dec., 2001.
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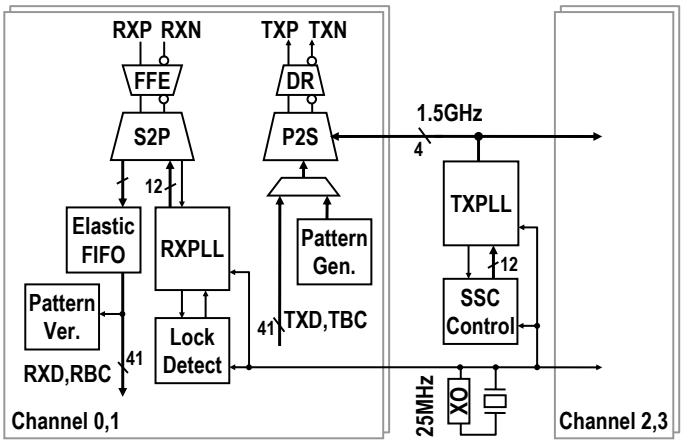


Figure 4.3.1: 6-Gb/s quad-channel configuration.

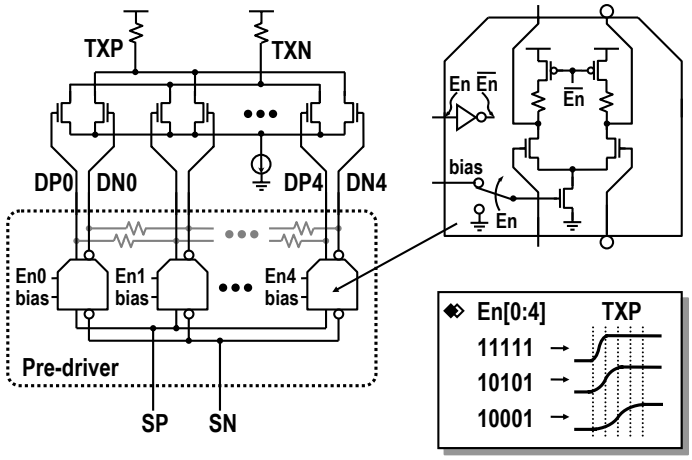


Figure 4.3.2: Programmable TX rise/fall time control.

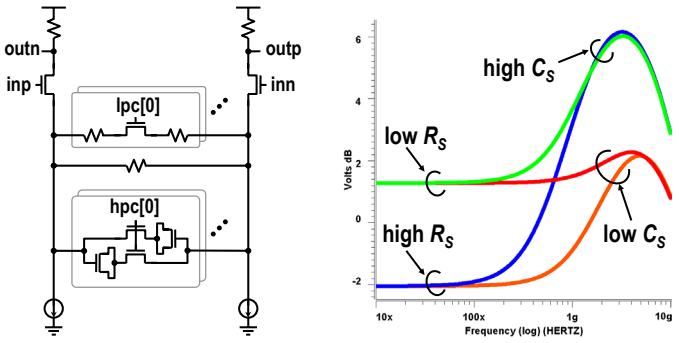
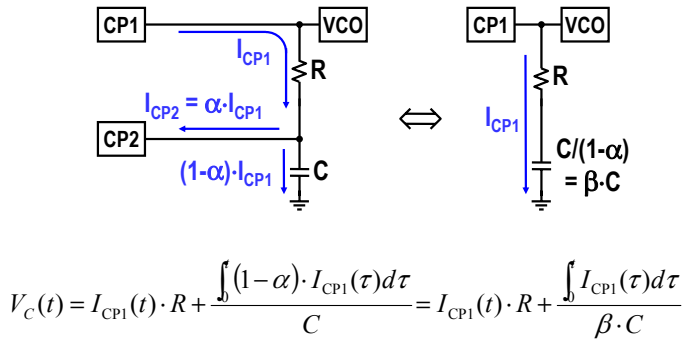
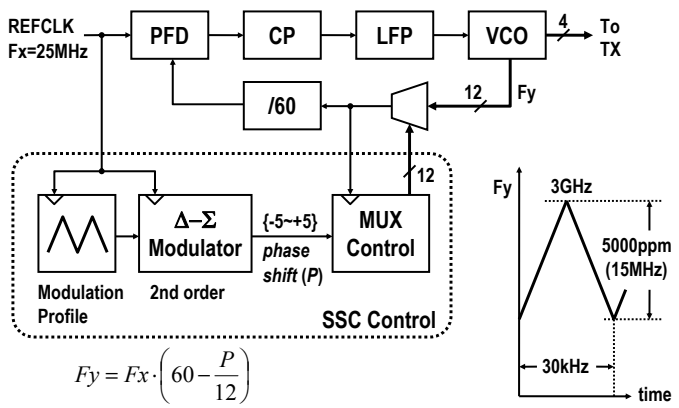


Figure 4.3.3: FFE with 0.25x varactor area.



$$V_C(t) = I_{CP1}(t) \cdot R + \frac{\int (1-\alpha) \cdot I_{CP1}(\tau) d\tau}{C} = I_{CP1}(t) \cdot R + \frac{\int I_{CP1}(\tau) d\tau}{\beta \cdot C}$$

Figure 4.3.4: Capacitance multiplication.



$$Fy = Fx \cdot \left(60 - \frac{P}{12}\right)$$

Figure 4.3.5: ΔΣ spread-spectrum clock generator.

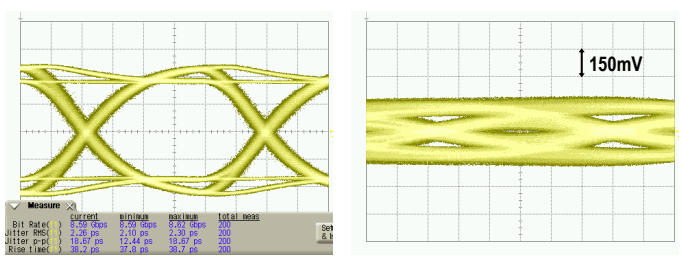


Figure 4.3.6: (a) 8.6Gb/s TX eye (b) 6Gb/s RX eye.

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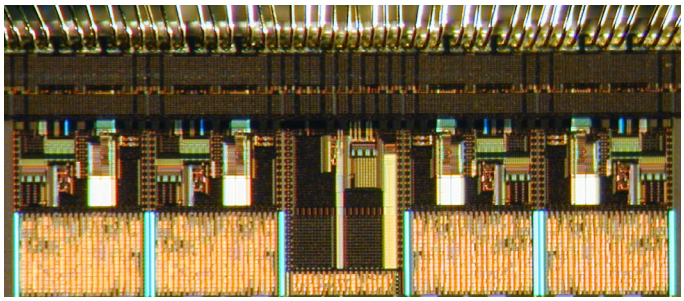

Figure 4.3.7: Chip micrograph.

